AMENDMENTS TO THE CLAIMS

List of Claims

1. (Currently Amended) A processing system including a processor, a main memory, and ~~an~~ a plurality of on-chip ~~cache~~ caches located on the same die as the processor, the caches being mapped to a plurality of main memory address ranges, respectively, and a corresponding one of the caches being configured to receive data from an address of the main memory upon a request for the data by the processor, the processing system comprising a crossbar interface between the processor and the on-chip ~~cache~~caches.

2. (Currently Amended) The processing system of claim 1 wherein the main memory is controlled by a memory controller, and the crossbar interface is configured to link the memory controller, the processor and the ~~cache~~caches.

3. (Currently Amended) The processing system of claim 1 wherein the crossbar interface comprises a plurality of ports via which the ~~cache~~ caches and the processor are linked based on the main memory address.

4. (Currently Amended) The processing system of claim 1 wherein the processor is configured to associate ~~at least one~~the plurality of main memory address ~~range~~ ranges with the ~~cache~~caches.

5. (Currently Amended) The processing system of claim 4 wherein the processor is linked with the ~~cache~~ caches based on ~~an~~ address ~~range~~ ranges stored in the processor and corresponding to ~~a~~ the range of addresses of the main memory respectively mapped to the ~~cache~~caches.

6. (Canceled)

7. (Currently Amended) The processing system of claim 1 ~~further comprising a plurality of caches~~, wherein the processor ~~comprising~~ includes an address range table ~~wherein~~ by which each of the address ~~range~~ ranges is associated with ~~a~~ one or more of the caches, respectively ~~cache~~.

8. (Original) The processing system of claim 7 wherein the address range table is programmable to change at least one of an address range and a cache associated with the processor.

9. (Currently Amended) The processing system of claim ~~1 further comprising a plurality of caches, the processor comprising a plurality of address ranges and~~7, wherein the table includes module identifiers corresponding to the caches.

10. (Currently Amended) The processing system of claim 9 1 wherein the crossbar interface comprises a plurality of ports, and the crossbar interface is configured to link ~~a~~ the caches ~~cache~~ with the processor via ~~a~~ ports, ~~port~~ associated with ~~an~~ the address ~~range~~ ranges in the main memory, respectively.

11. (Currently Amended) The processing system of claim 1 wherein the crossbar interface is configured to return the data requested by the ~~processor~~ processors to a corresponding one or more of the ~~cache~~ caches and the processor in parallel.

12. (Original) The processing system of claim 1 wherein the crossbar interface comprises at least one crossbar.

13. (Original) The processing system of claim 1 further comprising a plurality of processors linked with the cache via the crossbar interface.

14. (Currently Amended) A processing system comprising a plurality of processors on the same die, a main memory, a plurality of on-chip caches located on the same die as the plurality of processors, and a crossbar interface linking the on-chip caches and the processors, ~~each cache~~the caches being mapped to a plurality of main memory address ranges, respectively, and a corresponding one of the caches being configured to receive data from a range of the main memory upon ~~a request~~ an address for the data by one of the processors.

15. (Currently Amended) The processing system of claim 14 wherein at least two of the processors are configured to share at least one of the caches via the crossbar interface.

16. (Original) The processing system of claim 14 wherein the crossbar interface links one of the caches and one of the processors based on a module identifier supplied by the processor.

17. (Original) The processing system of claim 16 wherein the module identifier is associated by the supplying processor with a main memory address range.

18. (Canceled)

19. (Original) The processing system of claim 14 further comprising at least one memory controller configured to send data from the main memory to a receiving cache and a requesting processor at the same time.

20. (Previously Presented) A method for configuring a multi-processor processing system comprising the steps of:

providing a plurality of processors and a plurality of on-chip caches on the same die;

mapping a plurality of main memory address ranges to the plurality of caches;

mapping the caches to a plurality of processors; and

linking the processors and the caches using a crossbar interface.

21. (Original) The method of claim 20 further comprising the step of configuring a processor to interface with a cache to which is mapped a main memory address range addressable by the processor.

22. (Original) The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises associating, in a processor, a main memory address range with a module identifier for a cache.

23. (Original) The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises mapping a cache to more than one processor.

24. (Original) The method of claim 20 further comprising the step of changing a size of a cache, said step performed without changing the crossbar interface.

25. (Canceled)

26. (Original) The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises mapping more than one cache to one processor.

27. (New) The processing system of claim 14, wherein each of the processors is operable to configure a data request as including:

an identification of the processor making the request;

an identification of the cache to which the request is being made; and

an identification of the data being requested.

28. (New) The processing system of claim 14, wherein each of the caches is operable to configure, responsive to a cache hit, a return of data as including:

an identification of the cache returning the data;

an identification of the processor to which data corresponding to the cache hit is being returned; and

the data corresponding to the cache hit.

29. (New) The processing system of claim 20, the method further comprising configuring each request for data from the processors to include:

an identification of the processor making the request;

an identification of the cache to which the request is being made; and

an identification of the data being requested.

30. (New) The processing system of claim 20, the method further comprising configuring each data return from the caches to include:

an identification of the cache returning the data;

an identification of the processor to which data corresponding to the cache hit is being returned; and

the data corresponding to the cache hit.

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